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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/434,736	11/02/99	KIM S	000039-07360

020350
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MM91/0926

EXAMINER	
PERT,F	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 09/26/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)

1- File Copy

Office Action Summary	Application No.	Applicant(s)	
	09/434,736	KIM ET AL.	
	Examiner	Art Unit	
	Evan T. Pert	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-88* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12-28, 30-39, 41-43, 45-51, 55-56, 58-59, 64-76, 80, 83 and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in view of Gutierrez.

AAPA

A majority of the pending claim limitations are drawn to the prior art depicted in applicant's Figures 1A and 1B in U.S. Patent 5,683,938. AAPA sets forth a process and a device. The process and device of AAPA both involve a silicon substrate 1 with junction layer 2, gate oxide 4, gate electrode 5, conductive line on a second layer "spaced apart" 7, field oxide 3, first insulating layer 6, and second insulating layer 8.

The conductive elements (deemed "connection nodes" by the examiner) include the polysilicon gate electrode 5, junction layer 2 (which is P+ or N+ doped by Official Notice), and conductive line 7. AAPA teaches that these elements must be electrically connected to vias that rise upwardly to a common plane for interconnection wiring. In AAPA Fig. 1B, applicant teaches the prior art problem in that selective CVD fills the holes at the same rate such that the shallowest hole fills before the deeper holes.

The teachings of AAPA end here where applicant attempts to claim a solution thought of by Gutierrez:

Gutierrez

Gutierrez recognizes that it is better to fill holes of the same depth, by building up substantially "planar" conformal oxide insulating layers (230, 232, 234). Like applicant, Gutierrez teaches the advantage in using tungsten selectively deposited by gaseous deposition, when the substrate is silicon (self-seeding) [col. 3-5].

The examiner gives little regard to all of the limitations detailing the names of "connection nodes" as these are taught by AAPA. One of ordinary skill in the art would be fully aware of what elements need to be electrically interconnected and/or isolated in view of AAPA Figures 1A and 1B. Importantly, Gutierrez teaches nodes at every level of conformal oxide layers 230, 232 and 234. For example, the substrate nodes are contacted by vias 228 and 226 in the first insulating layer 230. Guttierez also teaches a conductive pattern 220 on the first insulating layer 230, which is then filled in tandem with via 224 that contacts the junction layer node. The concept of a "multi-level" metallization with a layer-by-layer filling of vias is clearly taught by Gutierrez.

Gutierrez does not textually teach contact holes with "tapered upper portions", or contact holes with an "upper portion width greater than a lower portion width" as claimed by applicant, but Gutierrez does clearly depict such contact holes in the cover Figure to his patent. For example, via 228 is on the first level and clearly has a "tapered upper portion" or "an upper width greater than a lower width". Indeed, looking to a variety of prior art, all contact holes can be considered to have some semblance of "taper".

It would have been obvious to adopt the teachings of Gutierrez pertaining to forming interconnects using "seed grown conductor" layers, particularly adopting tungsten with a silicon substrate since tungsten is self-seeded by silicon. Depositing in "one single step" is obvious in view of Gutierrez since he deposits in "one single step" when the substrate is silicon and the via metal is tungsten. Depositing in "one single step" at each level of oxide ILD (230, 232, 234) is a primary aspect of the invention of Gutierrez [col. 5, lines 25-38].

2. Claims 1, 3-6, 8-11, 52-54, 60-62, 77-79 and 85-87 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Gutierrez as applied to claims 15, 41 and 64 above, and further in view of Park taken with Erb.

Guttierez and AAPA are silent with respect to the shape of the contact holes, textually (but Guttierez does show taper pictorially where claim to a tapered "upper portion" does not preclude a tapered "lower portion").

There are many reasons one of ordinary skill in the art would want to modify the vertical vias of AAPA. For example, Erb teaches it is easier to align an upper metal deposit to a lower via by flaring out the metal of the lower contact 74, also achieving a compact fit to the target node 54. Alternatively, one of ordinary skill in the art might choose to create a "stepped portion" known as prior art in 1990, as is taught by Park [col. 1, lines 36-39]. This "stepped portion" is depicted in the Figures of Park, and is clearly formed by a combination of isotropic (wet) and anisotropic (dry) etching. The fact that Park is silent about how the "taper" is actually formed is merely evidence that the taper was common knowledge at the time of Park's filing.

It would have been obvious to create a stepped portion at the top of the vias in Guttierez by wet and dry etching, as is taught by Park (with elements of "wet" and "dry" clearly evident by Official Notice). One of ordinary skill in the art would be motivated to create a greater contact area to ease alignment as is taught by Erb.

3. Claims 2, 7, 57, 63, 82 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Guttierez, Park, and/or Erb as applied to claims 1, 6, 66 and 88 above, and further in view of Wolf.

Guttierez does not characterize his selective deposition of tungsten on silicon by gaseous precursor of tungsten fluoride as a "CVD" process. However, Wolf teaches the advantages of CVD tungsten in filling vias include better step coverage, selective deposition, and excellent electromigration resistance [Section 4.3.1.4, page 192].

It would have been obvious to characterize Guttierez's gaseous deposition method of tungsten into a via with silicon bottom as a "CVD" process. One of ordinary skill in the art would be motivated to use CVD tungsten for any of the reasons stated by Wolf on page 192.

Response to Arguments

4. Applicant has characterized "CVD" as "one single step" [last paragraph of page 24, paper no. 13].

5. Applicant has not explained how a straight "45° angle" can be formed in non-crystalline oxide insulating material with wet etch. However, applicant has clarified that "wet" and "dry" etching to get a tapered via "in the spirit" of the Figures was well within the skill of one of ordinary skill of the art. Rejections under 35 USC 112 are withdrawn.

6. The objections to the drawings are withdrawn since, as explained by applicant in Paper No. 13, these drawings are schematically representative, but are not exact. This is understood by applicant's response [page 25, last two paragraphs].

7. Applicant's arguments with respect to claims 1-88 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers can be reached on 703-308-2417. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ETP
September 24, 2001

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800